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## PATENT ABSTRACTS OF JAPAN

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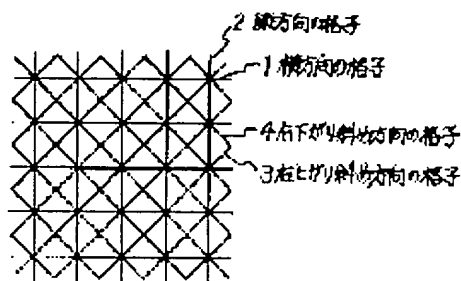
(72)Inventor : SATO AKIHIRO

## (54) AUTOMATIC LAYOUT METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT

## (57)Abstract:

PURPOSE: To make the length of wiring short by a method wherein, in addition to wiring layer which is used for wiring on lattices in the transverse and longitudinal directions in conventional cases, a wiring layer which is used for lattice-shaped wiring in the oblique direction is used.

CONSTITUTION: In addition to lattices 1 in the transverse direction and lattices 1 in the longitudinal direction, lattices 3 in the rightward ascending oblique direction and lattices 4 in the rightward descending oblique direction are set, they are used as wiring layers which are used mainly for wiring on the respective lattices 1, 2, 3, 4, and a first inter-connection layer to a fourth wiring layer are allotted. Thereby, the length of the wiring can be shortened to 0.7 times at the most, and the wiring resistance and wiring capacitance are reduced. As a result, the operating speed of the title integrated circuit can be made fast.



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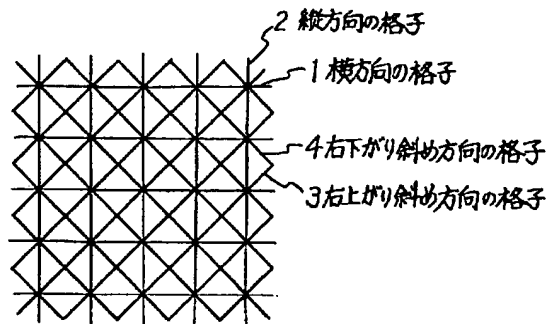
(54)【発明の名称】 半導体集積回路の自動レイアウト方法

(57)【要約】

【目的】 決められた格子の上を定められた配線層で配線するアルゴリズムを用いた半導体集積回路の自動レイアウト方法で配線した配線の長さを短かくする。

【構成】横方向の格子1および縦方向の格子2に加えて新たに斜め方向の格子3、4を設け、それぞれの格子上に主に使う配線層を定める。これにより配線すると、A点B点間の配線ボタン5、C点D点間の配線ボタン6のようになる。

【効果】配線の長さを最大0.7倍に短かくすることができ、配線抵抗と配線容量が減るので動作速度が速くなる。



## 【特許請求の範囲】

【請求項1】 少なくともひとつの横方向の格子上の配線に使う配線層と、少なくともひとつの縦方向の格子上の配線に使う配線層と、少なくともひとつの斜め方向の格子上の配線に使う配線層とを用いることを特徴とする半導体集積回路の自動レイアウト方法。

## 【発明の詳細な説明】

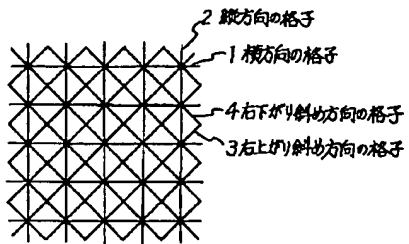
## 【0001】

【産業上の利用分野】本発明は半導体集積回路の自動レイアウト方法に関し、特に決められた格子の上を定められた配線層で配線するアルゴリズムを用いた自動レイアウト方法に関する。

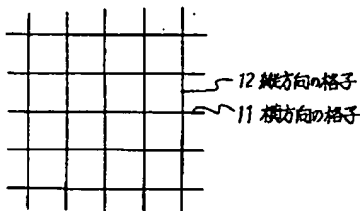
## 【0002】

【従来の技術】従来の決められた格子の上を定められた配線層で配線するアルゴリズムを用いた半導体集積回路の自動レイアウト方法は、例えば図3に示すように、第1の配線層を主に横方向の格子11上の配線に使い、第2の配線層を主に縦方向の格子12上の配線に使っていた。さらに、3層以上の配線層を使う場合は、第3の配線層を第1の配線層と同一の横方向の格子11上、第4の配線層を第2の配線層と同一の縦方向の格子12上、20 10 15 20 25 30 35 40 45 50 55 60 65 70 75 80 85 90 95 100 105 110 115 120 125 130 135 140 145 150 155 160 165 170 175 180 185 190 195 200 205 210 215 220 225 230 235 240 245 250 255 260 265 270 275 280 285 290 295 300 305 310 315 320 325 330 335 340 345 350 355 360 365 370 375 380 385 390 395 400 405 410 415 420 425 430 435 440 445 450 455 460 465 470 475 480 485 490 495 500 505 510 515 520 525 530 535 540 545 550 555 560 565 570 575 580 585 590 595 600 605 610 615 620 625 630 635 640 645 650 655 660 665 670 675 680 685 690 695 700 705 710 715 720 725 730 735 740 745 750 755 760 765 770 775 780 785 790 795 800 805 810 815 820 825 830 835 840 845 850 855 860 865 870 875 880 885 890 895 900 905 910 915 920 925 930 935 940 945 950 955 960 965 970 975 980 985 990 995 1000 1005 1010 1015 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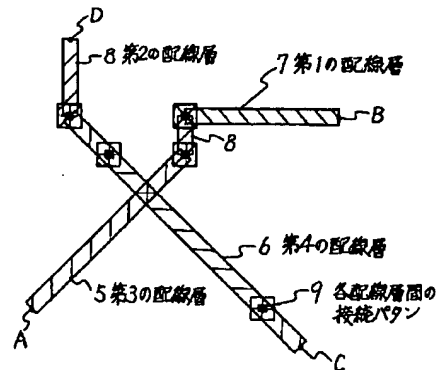
【図1】



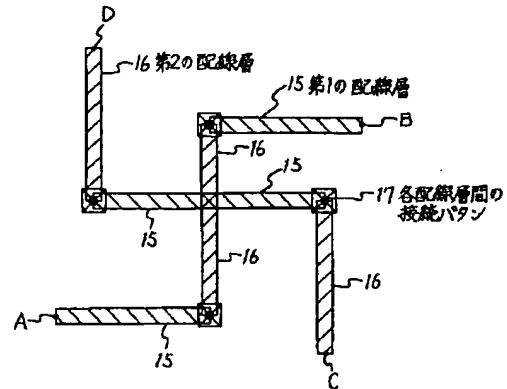
【図3】



【図2】



【図4】



フロントページの続き

(51)Int.Cl.<sup>5</sup>

識別記号

庁内整理番号  
7353-4M

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技術表示箇所

A

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(19) Japanese Patent Office (JP)

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(43) KOKAI Date: April 23, 1993

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(51) Int. CL. <sup>5</sup>	I.D. Symbol	Intern. Ref. No.	FI	Tech. Desig.
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G 06 F 15/60	370 P	7922-5L		
H 01 L 21/3205				
		9169-4M	H01L 21/82	W
		9169-4M		C
		7353-4M	H01L 21/88	A

Examination Request Status: Not yet requested

Number of Claims: 1 (Total 3 pages [in orig.])

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**(54) [Title of Invention]**

**Automatic Layout Method for Semiconductor Integrated Circuits**

**(57) [Abstract]**

**[Purpose]**

To shorten the wiring length of wiring made by an automatic layout method for semiconductor integrated circuits using an algorithm that implements wiring on decided lattice members in determined wiring layers.

**[Constitution]**

In addition to horizontal-direction lattice members 1 and vertical-direction lattice members 2, diagonal lattice members 3 and 4 are newly provided, and the wiring layer primarily used is determined on those lattice members. When wiring is implemented in this manner, the result is a wiring pattern 5 between point A and point B, and a wiring pattern 6 between point C and point D.

**[Benefits]**

It is possible to shorten the wiring length by a maximum factor of 0.7, whereupon wiring resistance and wiring capacitance are reduced so that the operating speed is increased.



## **[Claims]**

**[Claim 1]** An automatic layout method for semiconductor integrated circuits that employs a wiring layer using wiring on at least one horizontal-direction lattice member, a wiring layer using wiring on at least one vertical-direction lattice member, and a wiring layer using wiring on at least one diagonal-direction lattice member.

## **[Detailed Description of the Invention]**

[0001]

### **[Field of the Invention]**

This invention concerns an automatic layout method for semiconductor integrated circuits, and more particularly concerns an automatic layout method that uses an algorithm that implements wiring on decided lattice members in determined wiring layers.

[0002]

### **[Prior Art]**

In a conventional automatic layout method for semiconductor integrated circuits that uses an algorithm that implements wiring on decided lattice members in determined wiring layers, as diagrammed in Fig. 3, for example, a first wiring layer is primarily used in wiring on a horizontal-direction lattice member 11, while a second wiring layer is primarily used in wiring on a vertical-direction lattice member 12. Furthermore, when three or more wiring layers are used, [the additional layers] are allocated in sequence, the third wiring layer being made on the same horizontal-direction lattice member 11 as the first wiring layer, and the fourth wiring layer being made on the same vertical-direction lattice member 12 as the second wiring layer.

[0003]

Fig. 4 is a diagram of a pattern actually wired following the lattice diagrammed in Fig. 3. In Fig. 4, there are a first wiring layer 15 in the horizontal direction and a second wiring layer 16 in the vertical direction, with these wiring layers 15 and 16 being electrically connected by a connection pattern 17. These are wiring patterns for making electrical connections between points A and B, and C and D.

[0004]

### **[Problems Which the Present Invention Attempts to Solve]**

With a conventional automatic layout method for semiconductor integrated circuits such as this, wiring is only implemented on either a horizontal-direction or vertical-direction lattice member 11 or 12, even when using three or more wiring layers. Therefore, even when the number of wiring layers is increased, all that happens is that wiring is made easier, and wiring

length is hardly shortened at all, which constitutes a problem.

[0005]

An object of the present invention is to provide an automatic layout method for semiconductor integrated circuits wherein wiring length is shortened and the problem noted above is resolved.

[0006]

#### **[Means Used to Solve the Abovementioned Problems]**

The automatic layout method for semiconductor integrated circuits of the present invention is configured so as to employ a wiring layer using wiring on at least one horizontal-direction lattice member, a wiring layer using wiring on at least one vertical-direction lattice member, and a wiring layer using wiring on at least one diagonal-direction lattice member.

[0007]

#### **[Embodiments]**

Fig. 1 is a diagram of a wiring lattice used in a first embodiment of the present invention. In Fig. 1, in addition to horizontal-direction lattice members 1 and vertical-direction lattice members 2, diagonal-direction lattice members 3 that rise to the right and diagonal-direction lattice members 4 that decline to the right are established, and first, second, third, and fourth wiring layers are allocated as wiring layers used primarily in wiring on lattice members 1, 2, 3, and 4, respectively.

[0008]

Fig. 2 is a pattern diagram wherein a wiring pattern has been made using the lattice diagram of Fig. 1.

[0009]

In Fig. 2, there are a first wiring layer 7, a second wiring layer 8, a third wiring layer 5, and a fourth wiring layer 6, with an inter-wiring-layer connection pattern 9 provided at the connection points, etc.

[0010]

Fig. 2 shows an example of a wiring between point A and point B, and point C and point D. The wiring length is shortened by a factor of 0.7 to 0.8, compared to that of the conventional [wiring] shown in Fig. 4.

[0011]

### **[Benefits of the Invention]**

The present invention, as described in the foregoing, by using wiring layers used in wiring on diagonal-direction lattice members in addition to wiring layers used in wiring on the usual horizontal- and vertical-direction lattice members, can shorten wiring lengths by a maximum factor of 0.7, providing the benefits of reduced wiring resistance and wiring capacitance, and faster operating speeds.

### **[Brief Description of the Drawings]**

Fig. 1 is a diagram of a wiring lattice used with the automatic layout method for semiconductor integrated circuits in one embodiment of the present invention;

Fig. 2 is a diagram of a wiring pattern produced in conformity with the lattice diagrammed in Fig. 1;

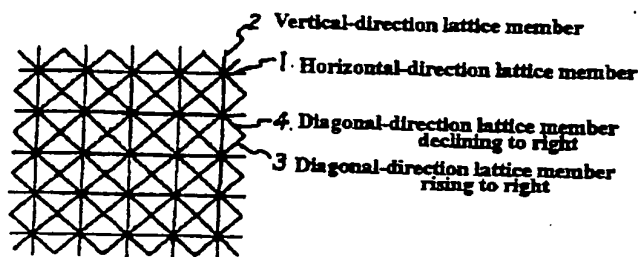
Fig. 3 is a diagram of a wiring lattice used in a conventional automatic layout method; and

Fig. 4 is a diagram of a wiring pattern produced in conformity with the lattice diagrammed in Fig. 3.

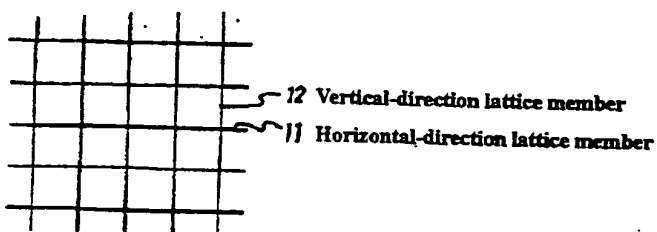
### **[Explanation of Symbols]**

- 1, 11 Horizontal-direction lattice members
- 2, 22 Vertical-direction lattice members
- 3 Diagonal-direction lattice member rising to right
- 4 Diagonal-direction lattice member declining to right
- 5, 6, 15, 16 Wiring patterns between two points

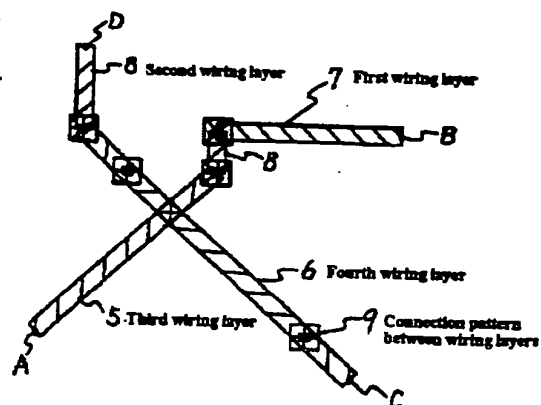
[Figure 1]



[Figure 3]



[Figure 2]



[Figure 4]

